AMENDMENTS TO THE CLAIMS

The following Listing of Claims replaces all prior versions and listings of Claims in the Application.

Listing of Claims:

Claim 1 (Currently amended): A link bus between control chipsets~~, said control chipsets including a first control chip and a second control chip, said link bus~~ comprising:

a first address/data (AD) bus for transmitting ~~address~~ addresses and data ~~chiefly~~ unidirectionally ~~from said first control chip to said second control chip~~ in a first unidirectional mode and in both directions in a first bidirectional mode; ~~and~~

a second address/data bus for transmitting ~~address~~ addresses and data ~~chiefly~~ unidirectionally ~~from said second control chip to said first control chip~~ in a second unidirectional mode and in both directions in a second bidirectional mode;

a first control chip coupled to said first address/data bus and said second address/data bus, said first control chip controlling transmission on only said first address/data bus in said first unidirectional mode and controlling transmission on both said first address/data bus in said first bidirectional mode;

a second control chip coupled to said second address/data bus and said first address/data bus, said second control chip controlling transmission on only said second address/data bus in said second unidirectional mode and controlling

transmission on both said second address/data bus and said first address/data bus in said second bidirectional mode;

a first command signal line for transmitting a first request signal to said second control chip from said first control chip, wherein said first control chip undergoes a transition from said first unidirectional mode to said first bidirectional mode only upon said second control chip receiving said first request signal while not transmitting on said second address/data bus; and

a second command signal line for transmitting a second request signal from said second control chip to said first control chip, wherein said second control chip undergoes a transition from said second unidirectional mode to said second bidirectional mode only upon said first control chip receiving said second request signal while not transmitting on said first address/data bus.

Claims 2 – 7 (Cancelled).

Claim 8 (Original): The link bus of claim 1, wherein said first control chip is a north bridge chip, and said second control chip is a south bridge chip.

Claim 9 (Original): The link bus of claim 1, wherein said first control chip is a south bridge chip, and said second control chip is a north bridge chip.

Claim 10 (Currently amended): A method for arbitration a link bus between control chipsets, said control chipsets including a first control chip, a second control chip, said link bus including a first address/data (AD) bus, and a second address/data bus, said method comprising:

transmitting ~~address~~ addresses and data through said first AD bus from said first control chip to said second control chip;

transmitting a request signal only over a first request signal line from said first control chip to said second control chip ~~when said first control chip needs~~ to request control of said second AD bus by said first control chip;

~~holding said second AD bus if said second control chip is still transacting through said second AD bus;~~ and

transmitting ~~address~~ addresses and data from said first control chip to said second control chip through said second AD bus ~~after a turn-around cycle~~ only if said second control chip ~~doesn't need~~ is not transmitting on said second AD bus at a time of receipt of said request signal.

Claim 11 (Currently amended): The method of claim 10, further comprising:

transmitting a request signal only over a second request signal line from said second control chip to said first control chip while said first control chip is transmitting on said second AD bus, ~~if~~ and said second control chip ~~needs~~ requires

said second AD bus~~, when said first control chip is transacting through said second AD bus~~;

ceasing transmissions ~~stopping transacting~~ through said second AD bus[[;]] from said first control chip; and

transmitting ~~address~~ addresses and data from said second control chip to said first control chip through said second AD bus ~~after a turn-around cycle~~.

Claim 12 (Original): The method of claim 10, wherein said first control chip is a north bridge chip, and said second control chip is a south bridge chip.

Claim 13 (Original): The method of claim 10, wherein said first control chip is a south bridge chip, and said second control chip is a north bridge chip.

Claim 14 (Currently amended): An arbitration method of a link bus between control chipsets, said control chipsets including a first control chip, and a second control chip, said link bus including a first address/data (AD) bus, and a second address/data bus, said arbitration method comprising:

controlling said second AD bus to transmit address and data from said second control chip to said first control chip;

transmitting a request signal only over a first request signal line from said second control chip to said first control chip ~~when said second control chip needs~~ to request control of said first AD bus by said second control chip;

~~holding said first AD bus if said first control chip is still controlling said first AD bus;~~ and

controlling said first AD bus to transmit ~~address~~ addresses and data from said second control chip to said first control chip ~~after a turn-around cycle~~ if said first control chip ~~doesn't need~~ is not controlling said first AD bus at a time of receipt of said request signal.

Claim 15 (Currently amended): The arbitration method of claim 14, further comprising:

transmitting a request signal only over a second request signal line from said first control chip to said second control chip while said second control chip is controlling said first AD bus, ~~if~~ and said first control chip ~~needs~~ requires said first AD bus~~, when said second control chip is still controlling said first AD bus~~;

relinquishing control of ~~stopping controlling~~ said first AD bus ~~from~~ by said second control chip; and

controlling said first AD bus to transmit ~~address~~ addresses and data from said first control chip to said second control chip ~~after a turn-around cycle~~.

Claim 16 (Original): The arbitration method of claim 14, wherein said first control chip is a north bridge chip, and said second control chip is a south bridge chip.

Claim 17 (Original): The arbitration method of claim 14, wherein said first control chip is a south bridge chip, and said second control chip is a north bridge chip.